U.S.S.N. 10/075,938

Claim Amendments

Please amend claims 1, 2, 4-9, 11, 12, 14, 16-19, 21 as follows:

Please cancel claims 10, 20 and 22 as follows:

Please add new claims 24 and 25 as follows:

Listing of Claims

1. (currently amended) A method for improving repairing efficiency in a non-volatile memory, said method comprising the steps of:

reading repairing data from an information array associated with said non-volatile memory to a volatile latch array associated with said non-volatile memory, said information array sharing a read circuit with a main memory array comprising said non-volatile memory; and,

~~providing a plurality of columns and rows associated with said non-volatile memory;~~

~~associating each of said plurality of columns associated with said non-volatile memory with a respective I/O terminal;~~

~~associating at least one spare column with at least two of each of said plurality of columns associated with both said non-volatile memory and with a respective I/O terminal; and~~

enabling an error correction coding circuit separate from said information array during reading of said repairing data including corrupted repairing data located anywhere in said information array, said repairing data for identifying and repairing defective columns or rows ~~associated with~~ comprising said ~~non-volatile memory~~ main memory array despite corruption of the repairing data as read.

2. (currently amended) The method of claim 1 further comprising the step of:

enabling said error correction coding circuit during an access of [[a]] said main memory array ~~associated with~~ comprising said non-volatile memory for correcting a correctable error if a particular address corresponds to an address of at least one defective column comprising said main memory array.

3. (previously presented) The method of claim 2 wherein said particular address comprises a Y-address corresponding to said at least one defective column.

4. (currently amended) The method of claim 1 further comprising the step of:

using a read circuit linked to said main memory array to read data from said main memory array and to transmit the read data to said error correction coding circuit;

said error control circuit being connected to said volatile latch array to permit data to be transferred from said error correction coding circuit to said volatile latch array;

said error correction coding circuit being linked to a decoder circuit and thereby to said information array, at least one spare row and said main memory array, and wherein said main memory array includes a normal array and at least one spare column.

5. (currently amended) The method of claim 4 ~~further comprising the step of:~~ wherein said volatile latch array is linked to said decoder circuit to thereby permit data contained within said volatile latch array to be accessed by said decoder circuit.

6. (currently amended) The method of claim 1 further where in the step of reading repairing data from an information array

associated with said non-volatile memory to a volatile latch array associated with said non-volatile memory~~,~~ further comprises the steps of:

accessing said repairing data contained within said information array following initialization of a computer system associated with said non-volatile memory; and

thereafter transferring said repairing data to said ~~non-volatile memory~~ volatile latch array.

7. (currently amended) A method for improving repairing efficiency in a non-volatile memory, said method comprising the steps of:

reading repairing data from an information array associated with said non-volatile memory to a volatile latch array associated with said non-volatile memory, said information array sharing a read circuit with a main memory array comprising said non-volatile memory;

~~providing a plurality of columns and rows associated with said non-volatile memory;~~

~~associating each of said plurality of columns associated with said non-volatile memory with a respective I/O terminal;~~

~~associating a spare column with at least two of each of said plurality of columns associated with both said non-volatile memory and with a respective I/O terminal; and~~

enabling an error correction coding circuit separate from said information array during reading of said repairing data including corrupted repairing data located anywhere in said information array, said repairing data for identifying and repairing defective columns or rows comprising said main memory array despite corruption of the repairing data as read; and,

enabling [[an]] said error correction coding circuit during an access of [[a]] said main memory array ~~associated with~~ comprising said non-volatile memory for correcting a correctable error at a particular address correspond[[s]]ing to an address of at least one defective column comprising said main memory array, wherein said particular address comprises a Y-address.

8. (currently amended) A method for improving repairing efficiency in a non-volatile memory, said method comprising the

steps of:

reading repairing data from an information array associated with said non-volatile memory to a volatile latch array associated with said non-volatile memory, wherein said repairing data is read utilizing a read circuit linked to a main memory array associated with said non-volatile memory and an error correction coding circuit separate from said information array linked to said volatile latch array and thereby to a decoder circuit, said information array sharing said read circuit with said main memory array; and,

~~providing a plurality of columns and rows associated with said non-volatile memory;~~

~~associating each of said plurality of columns associated with said non-volatile memory with a respective I/O terminal;~~

~~associating a spare column with at least two of each of said plurality of columns associated with both said non-volatile memory and with a respective I/O terminal; and~~

enabling said error correction coding circuit during reading of said repairing data including corrupted repairing

data located anywhere in said information array, said repairing data for identifying and repairing defective columns or rows comprising said main memory array despite corruption of the